AN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH 45nm FINFET TECHNOLOGY

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ABSTRACT

In this study, an operational transconductance amplifier is designed with 45nm FinFET technology process model. The low leakage current, low parasitic resistance and high current driving abilities of the SOI FinFET technology are taken into realization with a basic analog building block OTA circuit. The designed OTA circuit is tested in SPICE simulation environment with Level 57 process parameters. The simulation results are given and concluded.

I. INTRODUCTION

Due to their high immunity to short channel effects, importance of MOSFET with multiple gates (MUGFET) or FinFETs are increased by technologists for sub-100nm [1]. Especially for the digital applications, numerous FinFET realizations have reported with effective and improved feasibility, economy and performance with respect to up to date CMOS bulk technologies [2, 3, 6, 8]. Since, the FinFETs have better electrostatic channel control characteristic with improved turn off, they are considered as promising candidate for the future's fulfilling CMOS device demands [2].

In addition to excellent channel control, the FinFET transistors also offer approximately twice the on-current because of the two channels, even without channel doping. This is beneficial for the carrier mobility and results in a low gate leakage at the same time [7].

The Concept of device scaling has been consistently endorsed over the past few decades in meeting performance and power consumption requirements in VLSI circuits. Scaling to 45 nm node and below might necessitate the use of new processing steps or new device concepts such as FinFETs. High-performance SOI CMOS circuits, compatible with low-power low-voltage (LP/LV) and high-speed, ultra-large-scale-integration (ULSI) applications, have been repeatedly demonstrated on submicron devices [3].

However, conventional device structures such as bulk MOS transistors are approaching fundamental physical limits [2, 3]. As device dimensions shrink to submicron and below, the limits of conventional MOS structures are becoming more pronounced due to strong short-channel effects and quantum effect, causing the increase in performance to be limited. It is therefore, necessary to look for new device structures to sustain the growth of the VLSI industry in the nanoscale generations. Double-gate silicon-on-insulator (SOI) transistors can be a good technology choice for nanoscale circuits [1, 4].

SOI technology has demonstrated many advantages over bulk silicon technology, such as low parasitic junction capacitance, high soft error immunity, elimination of CMOS latch-up, no threshold voltage degradation due to body effect, and simple device isolation process [8].

Recently, double gate SOI structure has attracted particular attention due to its inherent robustness to short-channel effects and improved current drive capability. The advantages of SOI transistors come at the expense of an additional gate (back-gate), leading to high gate capacitance, dual leakage channels, and tricky front and back-gate coupling, which complicate circuit design.

In this work, the advantages of the SOI FinFET transistors are considered to be carried out for a FinFET based OTA circuit. The OTA realization has the low gate leakage current, low parasitic capacitance advantages of SOI technologies. The design is implemented with 45nm SOI FinFET Technology and tested in SPICE simulation environment with Level 57 SOI process parameters. The simulation results are given and concluded.

II. THE FINFET

SOI circuits consist of single-device islands dielectrically isolated from each other and from the underlying

substrate as in Figure 1. The lateral isolation offers more compact design and simplified technology than in bulk silicon, since there is no need of wells or interdevice trenches. On the other hand, the vertical isolation allows erasing of the word latch-up from the SOI dictionary [10].

For low off-current, bulk MOS-devices need sufficiently high channel doping, which degrades the carrier mobility. Moreover, good channel control and high on current demand for a thin gate dielectric. However, especially for low power applications, the gate leakage current through thermal oxide becomes unaccepted high for thicknesses approaching 2 nm. Therefore a nitride oxide or even a high-k-dielectric is required, which up to now suffers from reduced carrier mobility with respect to thermal oxide [2].

Double Gate (DG) SOI Devices

Regardless of the underlying device process, DG devices can also be classified in terms of their structure as in Figure 1, 2, 3. Typically the front and back gates of DG devices are connected together resulting in a 3-Terminal (3-T) device and the 3-T devices can be used for direct replacement of conventional single gate four terminal bulk CMOS devices.

In such technologies, one can choose to connect the back and front gates together or to control them separately while designing a circuit resulting in new circuit styles. Connected back and front gates 3-T provides a simple way of mapping circuits designed in single gate technologies to double gates technologies. 3-T configuration provides more ON current for transistors as well [8].

On the other hand, independent gate control can be used for designing new circuit styles. For example, back gate bias can be used to dynamically adjust the threshold voltage of the front gate to tune the power and performance requirement of a circuit. It can also be used for merging parallel transistors or driving non-critical transistors in single gate driven mode to reduce power dissipation.

One of the major advantages of using double gate transistors is the lower leakage current. The major leakage components in double gate devices are: (a) sub threshold leakage and (b) gate leakage. In double gate structures presence of two gates and ultra-thin body helps to reduce the Short-Channel Effect (SCE), which significantly reduces the sub threshold leakage current [8].

Lower SCE in DG devices and the higher driver current, due to two gates, allows the use of thicker oxide in DG devices compared to bulk-CMOS structures. This helps to reduce the gate leakage current. Moreover, lower SCE allows the use of lower body doping where the body can even be intrinsic, in DG devices compared to bulk-CMOS structure.

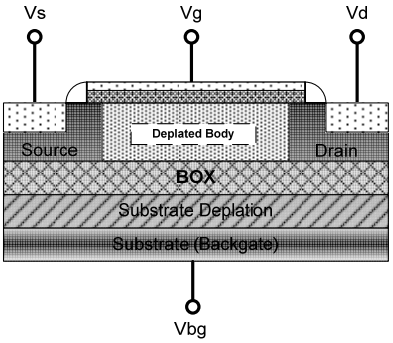

Figure 1. The SOI Layout

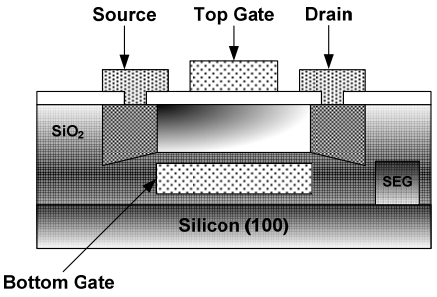

Figure 2. Layout of double gate SOI

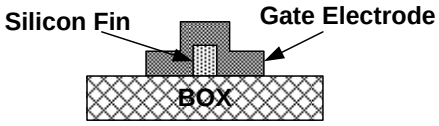

Figure 3. Layout of a FINFET

III. THE OTA CIRCUIT AND SIMULATION

An operational transconductance amplifier (OTA) is a voltage controlled current source. One of the first papers on OTA in the literature appeared nearly 38 years ago [15]. This paper described a bipolar OTA. At that time the emphasis was on amplifiers with feedback, such as op-amps.

In many analog or mixed VLSI applications, an operational amplifier may not be appropriate to use for an active element. For example, when designing integrated high-frequency active filter circuitry, a much simpler building block, called an OTA, is often used. More specifically the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal transfer characteristic is given below in equation (1) and (2).

$$I_{out} = g_m(V_{in+} - V_{in-}) \quad (1)$$

$$I_{out} = g_m.V_{in} \quad (2)$$

Where g_m is the transconductance, I_C control current, V_{in+}, V_{in-} and V_{in} are input voltages of OTA.

In this work, design of an operational transconductance amplifier with 45nm FinFET technology is attempted. Two gates of each FinFET are connected to each other. Schematic of proposed OTA circuit is given in figure 8. Characteristics graphs of such OTA are given in figures 4-7 respectively.

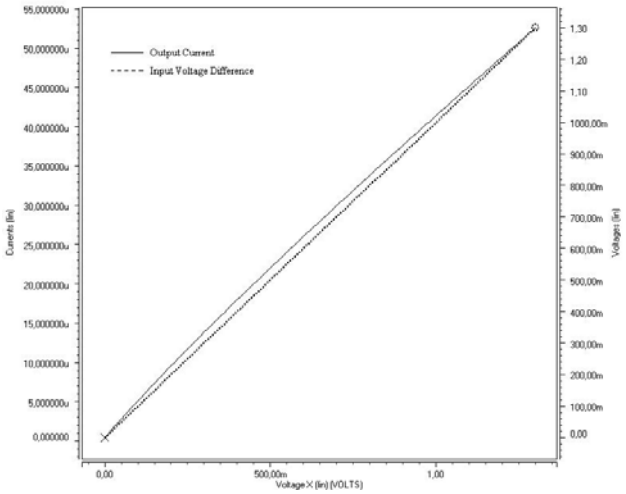

Figure 4.Output current vs. input voltage difference graph

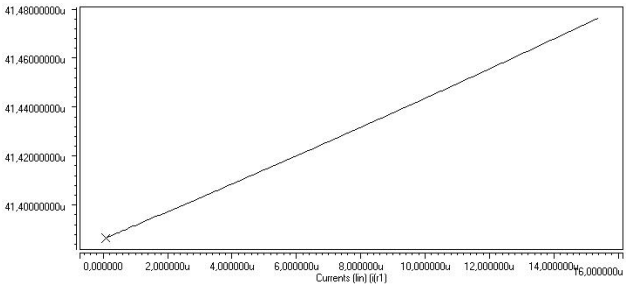

Figure 5. Control current vs. output current graph

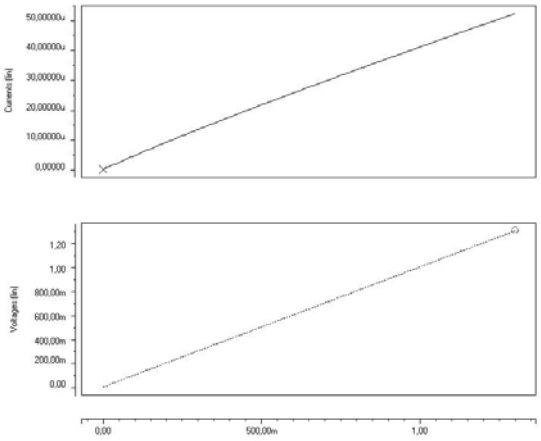

Figure 6. Output current vs. input voltage difference graph

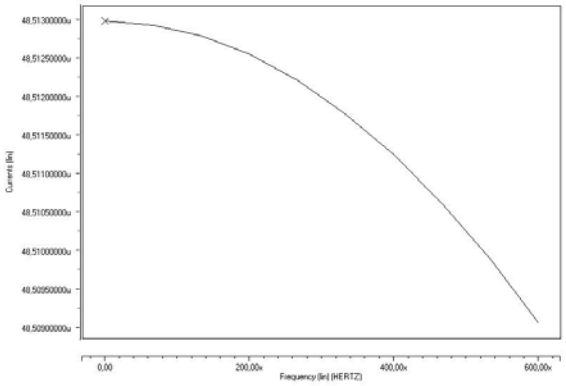

Figure 7 Frequency response of the OTA circuit

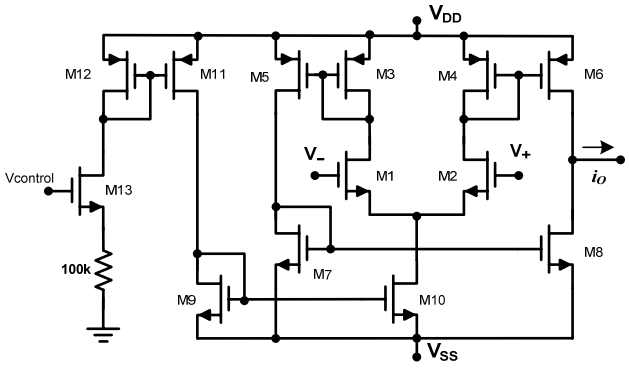

Figure 8.Schematic of the designed 45nm SOI OTA

The figures from Figure 4 to Figure 7 show DC, AC and control current versus output current characteristics of the OTA.

In Figure 4, the input voltage difference in equation (1) is x-axis and the output current is y-axis. Also to show the tracking efficiency of transconductance curve, input voltage difference put into the same graph. The second y-axis at the right hand side of Figure 4 is the same with the x-axis.

In Figure 5, the control current versus output current while the input voltage difference is kept constant 1 V. As seen from equation (2) and (3) if V_{in} = 1 V then the graph in Figure 5 directly gives K parameter in equation (3).

$$g_m = K.I_C \tag{3}$$

$$V_{in} = V_{in+} - V_{in-} \tag{4}$$

Equation (4) shows V_{in} and V_{in+} and V_{in-}. I_{out} is the output current.

Figure 6 is the separation of the two curves shown in Figure 4.

In Figure 7, the AC sweep simulation response is shown from 0 to 600 MHz. The maximum output current in the Figure 7 is 48.513 µA and the minimum current at 600 MHz is 48.509 µA. And the -3 dB point cannot be reached. Since the SPICE simulator does not support high frequencies or additional s-parameters are also required and it is not given by process only 600 MHz range has been used. According to this range any root cannot be reached as seen in Figure 7. As much as this knowledge, it is confirmed that, the SOI FinFET based realizations more advantageous with respect to bulk CMOS realizations about bandwidth and gain.

IV. RESULTS AND CONCLUSIONS

One of the basic analog building block OTA circuit is designed and simulated with SOI FinFET process technology in SPICE environment with level 57 parameters. The OTA circuit operated in a limited range. This is just a start of the FinFET based analog integrated circuit design. The high frequency range of the OTA circuits show that the FinFET SOI is a future candidate of current bulk CMOS technology. The proposed OTA circuit requires more improvements for the future works. Although this situation, the realization proves that the SOI FinFET technology can easily replace the circuits of current bulk MOS technology.

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