

Design and Performance Analysis of a Grid Connected PWM-VSI System

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Abstract

Pulse-width modulation (PWM) voltage source inverters (VSIs) are favorable interface devices to the power grid for renewable energy systems. This paper deals with the design of the LCL-filter and inverter for the grid-connected VSI. A complete design procedure for both reactive and passive components of LCL-filter is demonstrated with a new iterative approach in selection of the filter inductors. The design process for a two-level VSI is clearly illustrated through an example and the dynamic response is investigated under insufficient and sufficient damping cases. In this study, comprehensive analyses have been conducted to maximize the performance and efficiency. For this purpose, the line current total harmonic distortion (THD) and power factor performance of the designed system is assessed under various load conditions. Besides, the effects of the utilization of different PWM patterns on efficiency are compared and contrasted under different loads with altering switching frequencies. Simulation results validate theoretical findings throughout the design phase.

1. Introduction

Grid connected converters are increasingly being used due to the popularity of renewable energy systems. LCL line filters have proven to be useful on PWM switching harmonic attenuation and found to be favorable in comparison to the usual L filters in size and weight aspects. Especially in high power applications, where the switching frequency is limited to a few kHz, single L filters becomes bulky and costly. The use of LCL line filters brings the system to a more compact size and dynamic response of the converter is improved. Nevertheless, LCL-filter may lead to the amplification of undesired harmonic components around the closed loop stability boundary due to the presence of a pole pair at the resonant frequency (f_{res}) [1]-[3].

The damping of the LCL-filter can be achieved either passively or actively. Passive damping methods create a considerable amount of power loss for high power applications while the power loss due to passive damping is negligible for low power applications [3]. On the other hand, active damping methods could be used for low and medium power applications despite the complexity in the controllers [1]. Additionally, the existence of passive damping resistors modifies the LCL transfer function and degrades the advantages in harmonic suppression. Depending on the PWM switching method, harmonics around f_{res} of the LCL-filter may be produced unintentionally; however, the passive damping methods guarantee the stability of the converter.

As stated above, literature consists of plenty of researches about design and control of an LCL-filtered VSI and these

studies serve many methods for the damping of LCL resonance. Nevertheless, the designation of f_{res} is not elaborated in most of the articles except for [5]. This paper regards the determination of f_{res} as the key point of the design procedure since awareness of this frequency enables the designer to anticipate when damping is required to stabilize the system.

The goal of this paper is to embed f_{res} determination approach [5] in LCL-filter design procedure and convert the techniques of determination of the filter parameters in the literature into a straightforward method. However, the scope is not limited with LCL-filter design. Although, there are a variety of articles presenting LCL-filtered VSI design, none of them evaluates the design procedure under distinct PWM methods and switching frequencies. Additionally, literature has been still lacking a design methodology which performs efficiency, line current THD and power factor (PF) analyses under varying load conditions. In this paper, the design procedure includes efficiency, THD, and PF performance of the system under varying loads to assess the design quality unlike the design papers in this topic in the literature. Furthermore, the impacts of the preferred PWM switching patterns on efficiency are investigated with distinct switching frequencies along with FFT analyses of the line current (I_g) as supporting information. The verification of the designed LCL-filter together with the VSI is completed via simulation results.

2. System Modeling

The system analyzed in this paper is shown in Fig. 1. On the admittance transfer function between I_g and converter-side voltage of two-level VSI (V_c) in (1), equivalent series resistances (ESRs) of inverter-side inductance (L_c), grid-side inductance (L_g) and filter capacitance (C_f) are neglected and this assumption has no crucial effect on the analysis and provides a worst case scenario to reach stability.

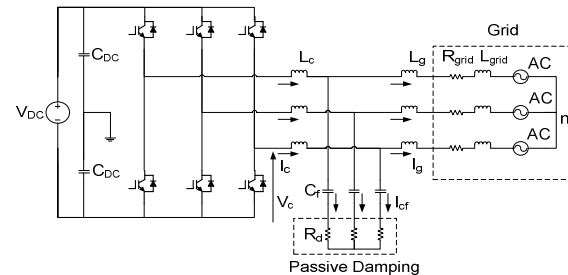


Fig. 1. Configuration of LCL-filtered VSI system

The reduction in switching ripple is targeted with the addition of a capacitor and a second inductor in contrast to a

standard L filter design. The high frequency ripple is filtered through the LC part. Low frequency fundamental current is not affected by the capacitive part; hence, the current controllers are designed as if there is not C_f present in the circuit.

The admittance transfer function between I_g and V_c derived in (1) represents the case when passive damping resistors (R_d) are used. So as to characterize the system when there is no passive damping, set $R_d=0$ in (1).

$$Y_{LCL}(s) = \frac{I_g(s)}{V_c(s)} = \frac{sC_f R_d + 1}{s^3 C_f L_c L_g + s^2 C_f R_d (L_c + L_g) + s(L_c + L_g)} \quad (1)$$

The resonant frequency, ω_{res} in rad/sec and the damping ratio (ζ) of the LCL-filter is determined as in (2) and (3) respectively.

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \quad (2) \quad \zeta = \frac{C_f \omega_{res} R_d}{2} \quad (3)$$

Although LCL-filters are superior to L filters in the aspects of PWM switching harmonics suppression, reduction of current ripple on the grid side and decrease in total size and weight, the control of the system becomes very complex due to the resonant pole pair created between the filter elements. Therefore, f_{res} plays a crucial role in the design procedure and resonance should be damped (with either active or passive damping methods) so that the system can reach stability. Only passive damping technique will be considered in this paper [1], [3].

Current controllers in the system use a rotating dq-frame synchronous to the grid frequency. Controller design is skipped in this paper, elaborated analysis on controller design is provided in [2], [4], and [7]. Current controllers use grid-side current feedback rather than converter-side current (I_c) feedback, as this approach provides superior control performance [7]. The design of LCL-filter parameters is investigated in detail in Section 3, through a step by step design procedure.

3. LCL-Filter Design

In literature, almost all of the LCL-filter design papers focus on either the total filter inductance in proportion to the base inductance value in p.u and/or utilize L_c calculation formulas by assuming reasonable ripple attenuation as the design criterion for the filter inductances. Nevertheless, these approaches make the design method weak. Since instead of designating f_{res} during the design phase, f_{res} is only checked whether to satisfy $10f_g < f_{res} < 0.5f_{sw}$ [1] condition at the very last step of the design phase. However, f_{res} must be set by the designer to rule the control actions properly. Thus, these approaches become limited and impractical for different power levels resulting in a trial-error process and could not provide a straightforward methodology. On the other hand, this paper includes the controllability action into the LCL-design phase and supplies a method for a variety of power levels with a straightforward approach. By doing so, the behavior of the designed system becomes foreseeable and stabilization turns into an easy task.

3.1. Step by Step Design

In this section, the LCL-filter design has been depicted in a step-by-step manner. The design process requires the power rating of the VSI (P_{rated}), DC bus voltage (V_{dc}), the grid frequency (f_g), switching frequency (f_{sw}), sampling frequency

(f_{samp}), and grid voltage (V_{grid}) in rms volts as inputs. The design algorithm is shown in Fig. 3 with the necessary inputs.

Selection of f_{res} lower than the critical frequency (f_{crit}) [5], [7] is adopted together with the grid-side current feedback throughout the LCL-filter design procedure. Therefore, damping of f_{res} is essential and passive damping technique will be used [7]. Furthermore, optimum damping control for LCL-filter resonance is another key issue. In order to achieve an adequate phase margin, a suitable crossover frequency for the filter should be determined. For this purpose, the zero dB gain crossover frequency (ω_c) must be fixed sufficiently below f_{res} [4], [5], and [7]. Selection of ω_c can be represented as $\omega_c = \alpha \omega_{res}$ and choosing $\alpha \leq 0.3$ provides phase margins higher than 50° ensuring system stability [4]. More information on the relation between ω_c and ω_{res} , is given in [4], [7]. Design steps are shown below in a consecutive manner according to the presented aims of the design phase.

Step-1: Firstly, determine the critical frequency in rad/sec (ω_{crit}) by using (4), where; T_{samp} is the sampling period (5).

$$\omega_{crit} = \pi / 3 T_{samp} \quad (4) \quad T_{samp} = 1 / f_{samp} \quad (5)$$

Note that the selected f_{res} should not be so close to f_{crit} since there is an uncertain and probably unstable region of operation at or near to f_{crit} [5]. In this case, the determination of the proportion of f_{res} to f_{samp} is the key point.

$$f_{crit} = \frac{\pi}{3} f_{samp} \frac{1}{2\pi} = f_{samp} / 6 \quad (6)$$

As can be seen in (6) f_{crit} is always 16.7% of f_{samp} . Therefore, selection of f_{res} as shown in (7) guarantees a region below f_{crit} which can be stabilized.

$$f_{res} / f_{samp} = 0.10 \sim 0.12 \quad (7)$$

Then, the condition in (8) must always be checked.

$$10f_g < f_{res} < 0.5f_{sw} \quad (8)$$

Note that f_{samp} is either equal to f_{sw} (single-update PWM) or twice of f_{sw} (double-update PWM); thereby, it has been proven that, with the procedure in this paper, f_{res} is always smaller than half of f_{sw} .

Step-2: In this step, the correlation constant (r) between L_c and L_g is defined as demonstrated in (9).

$$L_g = r L_c \quad (9)$$

It has been stated in [1] that maximum overall inductance of the LCL-filter depends upon the power level and application type. For instance, total filter inductance value should not exceed 0.1 p.u of the base inductance in low power applications so as to limit the ac voltage drop on inductors. However, for high power applications, sizes of the components become the primary concern of the designer. As the power ratings of the components increase, their size and cost also increase and cooling of these components becomes a tough issue which eventually degrades the efficiency. For minimum filter size, the total energy stored in the filter must be the smallest [3], [8]. Hence, for minimum filter size in high power applications, L_c and L_g must be selected to be the same, i.e. $r=1$ [3]. In addition, in [4] it has been recommended that L_g and L_c should be

selected equally in order to acquire maximum attenuation around switching harmonics.

(2) is re-organized as in (10) with the introduction of r .

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_c + rL_c}{rL_c^2 C_f}} = \frac{1}{2\pi} \sqrt{\frac{r+1}{rL_c C_f}} \quad (10)$$

Subsequently, (10) is used to calculate $L_c * C_f$ multiplication since f_{res} was determined in Step-1 and r was picked with filter size design criterion. After obtaining $L_c * C_f$ value, C_f can be calculated by using (11) and then L_c value is acquired. C_f is shown as the multiplication of reactive power absorption (x) by the capacitor and base capacitance (C_b) in (11). In general, C_f is limited to 1-5% of C_b to prevent excessive reactive power flowing into it. By doing so, PF decrease on the grid side is limited to 5%. Thus, x value is varied from 0.01 to 0.05 with relative small steps as in Fig. 2 (a) and gives corresponding L_c values until $\alpha \leq 0.3$ condition is satisfied. ω_c differs for each combination of C_f and L_c values as depicted in Fig. 2 (a), and the values fulfilling $\alpha \leq 0.3$ requirement are selected as the optimum filter parameters. The region determined by α is demonstrated in Fig. 2 (a) to visualize the selection range.

$$C_f = x * C_b = x * \frac{P_{rated}}{3 * 2\pi f_g * V_{grid}^2} \quad (11)$$

Step-3: In this step, the current ripple attenuation from inverter side to grid side is checked. To calculate the ripple reduction, at high frequencies inverter side is considered as a harmonic generator whereas grid side is modeled as short circuit [1]. The inverter side current ripple can be calculated with the formula in (12) provided in [8]:

$$\Delta i = \frac{V_{dc}}{8L_c f_{sw}} \leq \left(\frac{\text{Ripple \%}}{100} \right) * \hat{I}_{rated} \quad (12)$$

Inverter side current ripple (Δi) percentage should be limited in the range of 10-25% of the peak rated output current ($\hat{I}_{rated}$) [8]. The relationship between the harmonics generated by the inverter and injected into the grid is shown in (13).

$$\frac{i_g(h_{sw})}{i_c(h_{sw})} = \frac{1}{|1 + r(1 - L_c C_b \omega_{sw}^2 x)|} \quad (13)$$

The main objective of the LCL-filter design is to achieve 20-25% current ripple attenuation with respect to Δi . Therefore, total attenuation of the LCL-filter becomes $\Delta i(\%)$ (which is 10%-25%) times 20-25% attenuation provided by $L_g C_f$ part resulting in 2-5% attenuation in total.

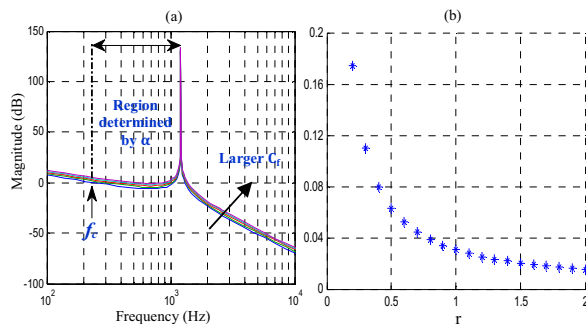


Fig. 2. (a) Bode plots of LCL-filters under various C_f
(b) $i_g(h_{sw})/i_c(h_{sw})$ vs. r

If the total attenuation of LCL-filter is not sufficient, either r value may be increased (Fig. 2 (b)) or Δi can be decreased by increasing f_{sw} until the desired attenuation is reached. However, increase in r makes the filter become too costly [1].

Step-4: At f_{res} , the impedance of the LCL-filter becomes zero and magnitude response tends to go to very large values at that frequency. Therefore, R_d 's should be added in series with C_f 's to provide non-zero impedance to limit the resonance peaks. Generally, the impedance of R_d should be at least one third of the impedance of C_f at f_{res} as in (14), [8]. Nevertheless, utilization of (3) to find R_d delivers the best approach. Determine ζ being at least 0.5 to provide sufficient damping. Generally, the optimum value of ζ is 0.707 for proper damping; however, it is recommended that ζ should be selected around 0.5 to limit damping losses at high power units [4].

$$R_d \geq \frac{1}{3\omega_{res} C_f} \quad (14)$$

Step-5: Verify the design under varying load conditions and f_{sw} . Before proceeding with design example, LCL-filter design algorithm is summarized in a flow diagram in Fig. 3 and all of the input data and calculated filter parameters by following the design algorithm in Fig. 3 are tabulated in Table 1.

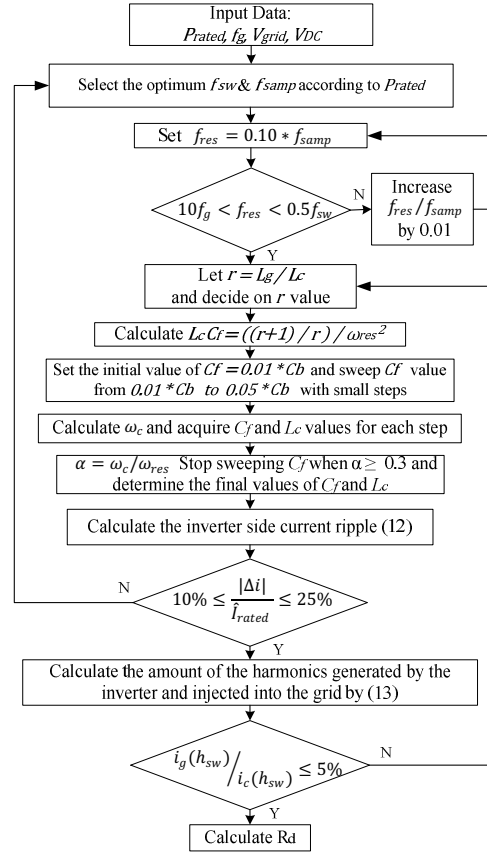


Fig. 3. LCL design algorithm

In the designed system, the preferred PWM pattern is space-vector PWM (SVPWM) and PWM mode is double update unveiling f_{smp} (control frequency) twice of f_{sw} . Modulation index, M_i convention in Table 1 is adopted as in [6].

Table 1. Specifications of LCL-filter system

f_{sw}	Switching Frequency	5 kHz	V_{dc}	DC Bus Voltage	1070 V
f_g	Grid Frequency	50 Hz	P_{rated}	Rated Power	250 kW
f_{samp}	Sampling Frequency	10 kHz	L_c	Converter Side Inductor	243 μ H (11.93%)
V_g	Grid Phase Voltage	400 V_{rms}	C_f	Filter Capacitance	145 μ F (2.92%)
M_i	Modulation Index	0.679	L_g	Grid Side Inductor	243 μ H (11.93%)

In the design algorithm f_{res} was determined at 1.2 kHz ($0.12 \cdot f_{samp}$). Besides, $\Delta i / \hat{I}_{rated}$ was found to be 0.15 ($\approx 15\%$) satisfying the diamond shaped constraint in Fig. 3. Subsequently, the current ripple injection from inverter side to grid side had to be determined with the help of (13). In Fig. 2 (b), for various r values, ripple attenuation amounts were plotted. As r was selected to be 1 throughout the design phase, corresponding attenuation in Fig. 2 (b) becomes approximately 0.03 (3%), injecting 3% of $\Delta i / \hat{I}_{rated}$ (15%) to the grid. Thus, total attenuation extent (0.45%) of the filter is satisfactory. As the final step, R_d calculation formulas presented in (3) and (14) showed the R_d values as $R_d = 0.9 \Omega$ ($\zeta = 0.5$) and $R_d \geq 0.305 \Omega$ respectively. Thus, R_d and ζ values will be verified to be sufficient with the aid of MATLAB in section 3.2 and final R_d value will be determined.

3.2. Simulation Results

In this section, the assessment of the design procedure is conducted via simulation software and mathematical tools by using the system specifications together with the calculated LCL-filter parameters listed in Table 1. For $R_d = 0.3 \Omega$ as found in Step-4 by using (14), simulated waveforms are shown in Fig. 4 (a), where serious transient oscillations occur at the transition from light load condition (10%) to full load condition deducing that the system is not damped sufficiently and this oscillations are very likely to unveil instabilities. Therefore, R_d should be increased in order to damp oscillations properly. As also found in Step-4 by using (3) $R_d = 0.9 \Omega$ may supply a sufficient damping. Hence, the amount of R_d to be augmented is verified by means of MATLAB. In Fig. 5, R_d values are varied from 0 to 2 Ω with 0.1 Ω steps. It has been inferred in Fig. 5 that to reach at least $\zeta = 0.5$, R_d ought to be picked as 0.9 Ω . If more damping is desired in the design, the value of ζ should be selected as the optimum value 0.707. Nevertheless, in this case there emerge a trade-off between the increasing losses and stability enhancement. With $R_d = 0.9 \Omega$, simulated waveforms in Fig. 4 (b) seem to be damped sufficiently and they are well-regulated both in the steady-state and transient conditions.

The next step is the FFT analysis of I_g of the designed system in Fig. 1. According to IEEE 519-1992 regulations, the magnitudes of the harmonic components starting from 35th and above should be lower than 0.3% of the magnitude of rated I_g . Therefore, the harmonics at f_{sw} and at its multiples should be monitored carefully. In Fig. 6, the harmonic components at 5 kHz (f_{sw}) constitute at most 0.19% of the rated I_g verifying that system is safe and damped appropriately.

In Fig. 7, THD percentage of I_g under varying load conditions is depicted. It can be inferred that harmonics injected to the grid is low enough even at light loads and as load increases I_g tends to become a pure sinusoidal wave. Furthermore, the deviation of the PF from unity with the change of load is also shown in Fig.

7. The change in PF is very tiny meaning that q-axis current controller functions properly owing to the grid-side feedback.

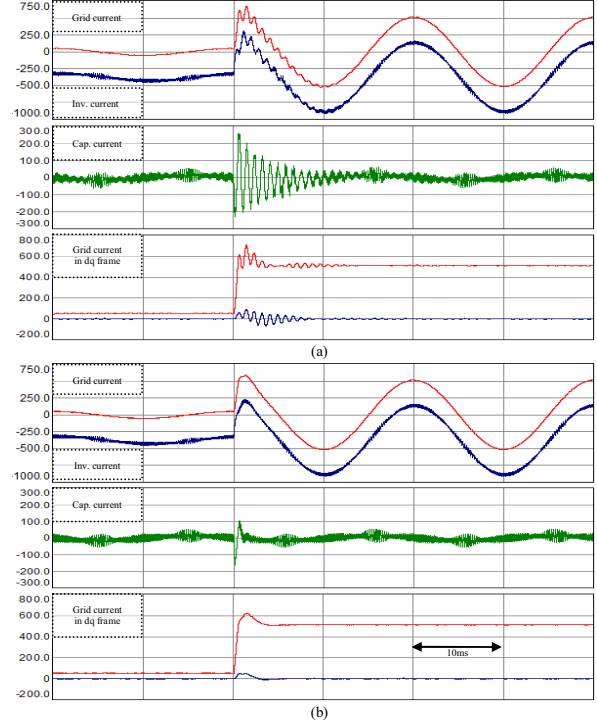


Fig. 4. Simulated results of LCL-filter based inverter using (a) $R_d = 0.3 \Omega$ and (b) $R_d = 0.9 \Omega$

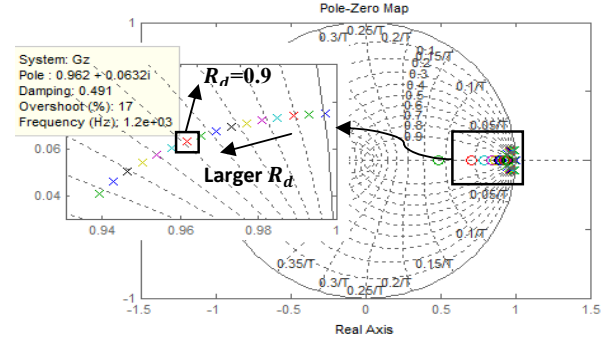


Fig.5. Poles & zeros of the open loop system with various R_d

The success of the two-level VSI design is mostly assessed with its efficiency performance. Damping losses together with the switching and conduction losses of semiconductor modules (IGBT) constitutes the main loss mechanisms in the system. With proper selection of IGBT modules and damping resistors, total loss of the VSI can be calculated. At this point, the effect of the selected PWM pattern is also considered briefly.

As the modulation pattern, discontinuous PWM methods are generally preferred rather than continuous methods. Since discontinuous PWM patterns provide low harmonic distortion and very low PWM ripple compared to continuous PWM patterns resulting in mitigation of the switching losses. Therefore, discontinuous-PWM1 (DPWM1) is compared with SVPWM in Fig. 8 concerning efficiency percentages with

regard to the corresponding loss calculations for each case. Note that increasing f_{sw} by 50% and employing DPWM1 method, the switching count i.e. switching losses remain the same while ripple of DPWM1 becomes less compared to SVPWM [6]. As can be seen in Fig. 8, DPWM1 method provides better efficiency characteristics than SVPWM at same f_{sw} especially at rated load conditions.

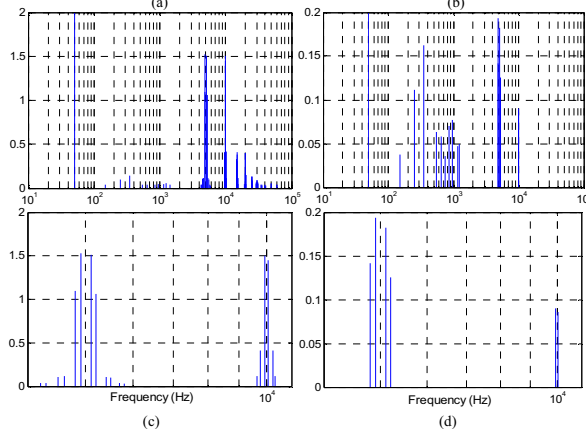


Fig. 6. THD percentages (%) vs. frequency of (a) I_c (b) I_g (c) I_c zoomed in f_{sw} and $2f_{sw}$ (d) I_g zoomed in f_{sw} and $2f_{sw}$ (THD of $I_c=3.60\%$ and $I_g=0.44\%$)

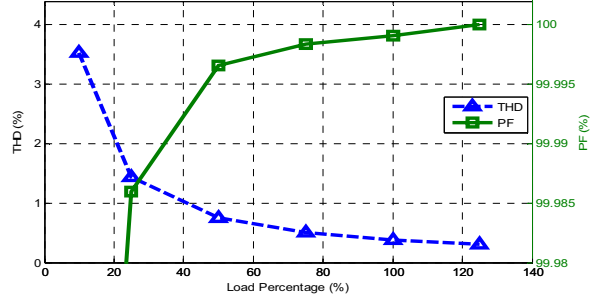


Fig. 7. THD and PF change vs. varying load conditions

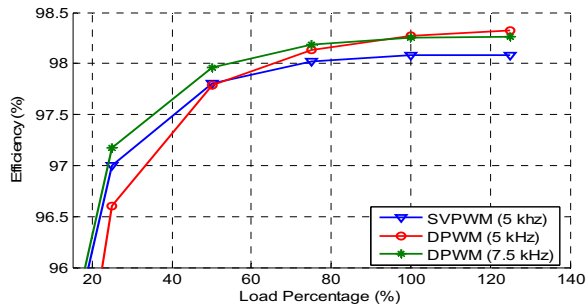


Fig. 8. Efficiency change vs. load percentage

Although employment of DPWM1 reduces the conduction losses significantly, the damping losses are increased compared to SVPWM at $f_{sw}=5$ kHz. FFT analysis in Fig. 9 reveals that magnitudes of the harmonic components at the side-bands of f_{sw} in DPWM1 case are much higher than magnitudes of the harmonics centered around f_{sw} in SVPWM causing almost twice higher damping losses at 5 kHz. Consequently, damping

losses are more dominant at light loads and SVPWM is favorable to DPWM1 in efficiency aspect at $f_{sw}=5$ kHz. Nevertheless, as the load increases conduction losses escalate and prevail over damping losses. Thus, DPWM1 shows better performance at half and higher loads compared to SVPWM.

DPWM1 method is also implemented by augmenting f_{sw} by 50% shown with DPWM1 (7.5 kHz) label in Fig. 8 and 9. Although the rise in f_{sw} increases IGBT switching losses, the damping losses are decreased compared to DPWM1 (5 kHz) and SVPWM cases as can be seen in Fig. 9 with the reduction in magnitudes of the harmonic content of I_c . Hence, efficiency performance is improved in DPWM1 (7.5 kHz) case although f_{sw} has been increased. To conclude, utilization of DPWM1 method at 7.5 kHz has provided the best efficiency performance.

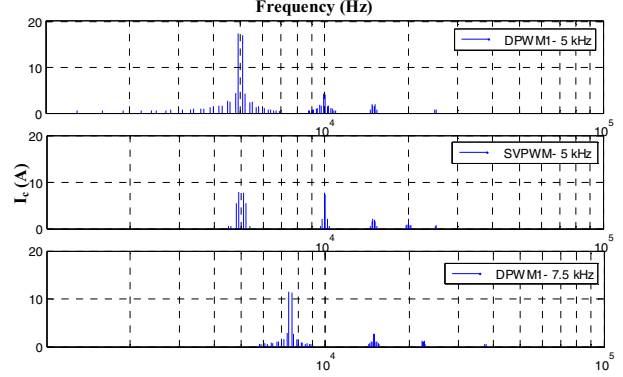


Fig. 9. The magnitudes of harmonic content of I_c under distinct PWM methods and carrier frequencies (f_{sw})

4. Conclusions

This paper analyzed the design of a VSI with an LCL-filter connected to the grid to reduce the frequency ripple. A complete design procedure for LCL-filter is demonstrated with a new step-by-step approach via flow diagram to calculate the required inductance of the filter. Design procedure does not only contain LCL-filter design, but also examines efficiency, THD and PF analyses under various load conditions. Moreover, the effects of the utilization of DPWM1 and SVPWM methods on efficiency have been evaluated under different loads with altering switching frequencies. The verification of the design method has been completed via simulations. The stability and the dynamic response of the designed system are analyzed considering the sufficiency of the damping of the resonant poles. A further design criterion for VSIs including the controller design is stated in detail in [7] as the complementary study of the LCL-filter design procedure presented in this paper.

5. References

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